

DFT (Design for Testability) Pattern Generation Task for Circuit Under Test

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Abstract— In this paper, we will present a method to reduce the power consumption during testing of a circuit-under-test (CUT). In proposed scheme the power reduced in two steps. In first step power reduced using gated clock design approach and in second step reduces the no of reduces the number of transitions at the inputs of the circuit-under-test.

Keywords- LFSR, Clock gating, Bit swapping, Bilt-in-self-test

I. INTRODUCTION

Power Dissipation is one of the most crucial considerations in designing a VLSI system. The main requirement for considering power during test is that power and energy are considerably higher in test mode than in system mode. The power consumption during test can be as higher as 200% of the power consumption in normal mode. Power dissipation of a system in test mode is more than that in normal mode because a significant correlation exists between the consecutive test vectors applied during the circuit's normal mode of operation, whereas this may not be necessarily true for applied test vectors in test mode of operation. Low correlation between test vectors increases switching activity and eventually leads to power dissipation in the circuit.

Built-In Self Test (BIST) is the popular approach for low power testing as it provides a larger scope for low power techniques to be used. BIST uses an LFSR as test pattern generator (TPG) and LFSR generates all possible test vectors with the proper use of tap sequence. Furthermore the pseudorandom behavior of the LFSR reduces the correlation among test vectors which means that it can achieve high fault coverage in a relatively short run of test vectors.

Hardware implementation of the PRBGs is almost always made up of the well-known linear-feedback shift register (LFSR) [1], whose generic circuit is reported in Fig. 1. This circuit is very simple to be implemented, but since the clock-path of all flip-flops (FFs) toggle at every clock cycle, they consume a significant amount of power. This problem was extensively addressed in [2] and, attenuate in [3], by implementing a parallel LFSR and adopting an efficient switch minimization procedure. Moreover, a further efficient low-power solution has been recently proposed in [4]. Although these solutions reduce power consumption, the obtained circuits are very complicated and they strongly increase the number of the total transistors and, consequently, the silicon area, thus obviating the major advantage provided by LFSRs.

In this paper, we present the gated clock design approach for LFSRs which can lead to power reduction without unduly complicating the traditionally simple topology. The analysis demonstrated that the power reduction hardly depends on the technological characteristic of the gates employed. Finally, the real efficiency of the presented gated-clock design should be evaluated also considering the increased silicon area required to implement the gating circuit.

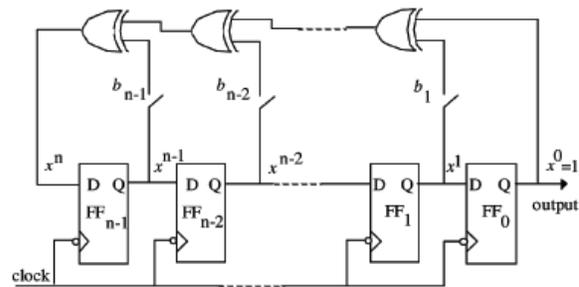


Figure 1. Simplified circuit of a generic n-bit LFSR.

II. CONVENTIONAL LFSR

Pseudo Random binary sequences are useful in many areas of digital design and science. Among these are encryption, CDMA code generation, and verification and maintenance of digital devices. LFSR is the most common used topology to implement PRBG. As shown in Fig. 2, it is obtained with an array of FFs with a linear feedback performed by several XOR gates. Although LFSRs are very simple to implement, they are based on a rather complex mathematical theory [5]. A 3-stage LFSR is characterized by its feedback polynomial [1], [7], [5] given by [6]

$$P(x) = 1 + x^2 + x^3 \dots (i)$$

However, they can be efficiently describes through the nth-order polynomial (1) where the binary coefficients define the well-known polynomial characteristic which the generator main properties depends

The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it

must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle

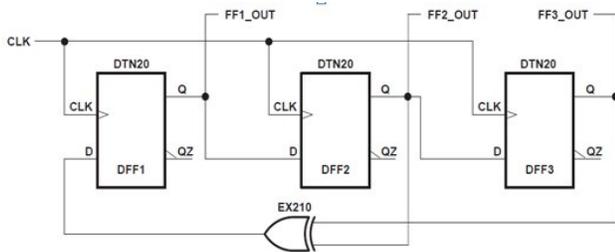


Figure 2 Three bit Conventional LFSR

Data_in	Data_out	Clock	Modified clock
1	0	1	1
0	1	1	1
1	1	1	0
0	0	1	0

Figure 3 Modified Clock

III. PROPOSED ARCHITECTURE

In BIST, the linear feedback shift register (LFSR) is mostly used to generate test patterns due to its low area and simple circuit. If a conventional LFSR is used as a test pattern generator, power consumption is significantly higher. To reduce power consumption during test, the new Architecture is proposed.

In the proposed approach, power consumption is reduced in two steps.

- Modified clock scheme
- Bit-swapping technique

In modified clock scheme, To reduce power consumption in a digital system a set of strategies termed dynamic power management (DPM) is often used. The DPMs strategy consists in disabling the logic circuits that are not performing functional operations during a particular time frame, thus reducing power consumption. At circuit level, this strategy is applied by the so-called “gated clock” approach which disables the clock of FFs [7]. More specifically, for FFs without an enable signal, which is our case, we can adopt the strategy proposed in [7] and modified in [8], [9] as it is shown in Fig. 2. This is done by activating the FF only when the input signal is different from the actual output value. As it can be easily understood, this approach is perfectly compatible with a LFSR only adding some extra gates, as shown in Fig. 3.

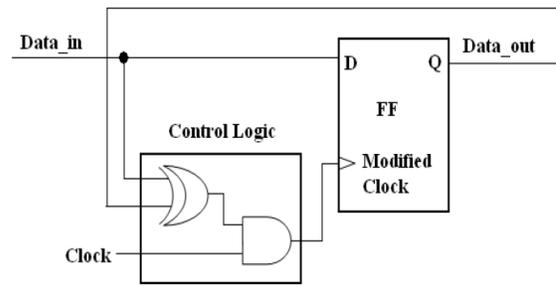


Figure 4 Switching unit of LFSR with Modified Clock

It is worth noting that the XOR and the NAND gates used to implement the gating can be implemented as a single gate (from hereinafter called XORNAND gate) as shown in Fig. 4. This is due to the complementary output always available in every FF. To analytically evaluate the power consumption of the gated clock approach applied to a LFSR, we have to take into account also the dissipation introduced by the extra gates that are employed to implement the gated clock circuits, as well as the load effects introduced by these gates with respect to the traditional one.

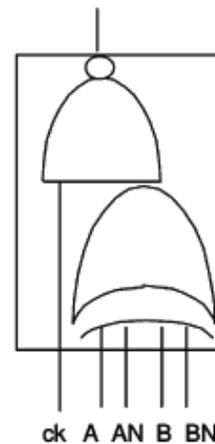
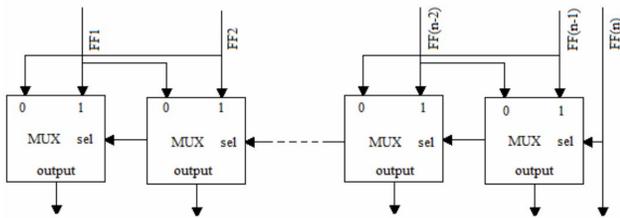


Figure 5 XORNAND CMOS schematic at gate level.

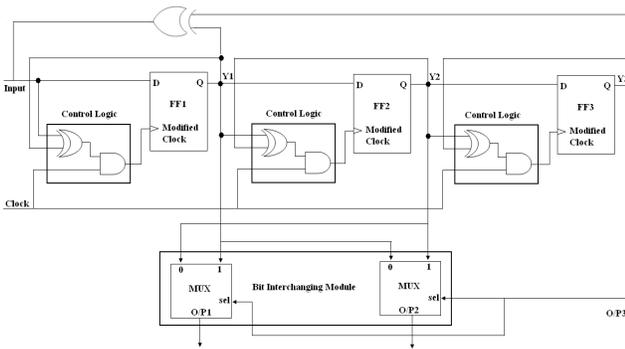
In bit swapping technique, The proposed design is based on reducing the number of transitions between consecutive test vectors generated by a conventional LFSR and applied to a CUT. If an n-bit maximal length LFSR starts with a non-zero seed and runs for 2n clock cycles to generate all possible test vectors, it will produce a number of transitions equal to 2(n-1) transitions at the output of each LFSR cell [3]. We modify the LFSR by considering one of its outputs (say bit n) to be a selection line that will swap two neighbouring bits elsewhere in the LFSR when the selection line has a specific value (say 0). So if n is odd and bit n / 4 0, then bit 1 will be swapped with bit 2, bit 3 with bit 4, . . . , bit n/2 with bit n/2 + 1. If n is even and bit n / 4 0, then bit 1 will be swapped with bit 2, bit 3

with bit 4, . . . , bit n-2 with bit n-1. In all cases the selection line, bit n in this case, is excluded from the swapping operation. If bit n = 1, then no swapping is performed. For this modified LFSR: 1. The exhaustive set of generated test vectors will be the same as the test vectors generated by the corresponding unmodified LFSR, but their order will be different. 2. Each pair of neighbouring bits that are swapped will save a number of transitions equal to $T_{saved} = \frac{1}{4} 2^{(n-2)}$. Since these two bits originally produce $2^{(n-1)}$ transitions, the bit swap will therefore save $T_{saved} = \frac{1}{4} 2^{(n-2)} / (2^{(n-1)}) = 25\%$. The above description assumes an external LFSR. It generalizes readily to internal LFSRs if the neighbor is defined as a pair of cells where the output of one feeds the input of the other directly (i.e. without an intervening XOR gate).

Based on the suggested modification above, the modified LFSR can be designed using the conventional LFSR and a group of two-input multiplexers as shown in Fig. 1, where bit n is considered as the selection line of the multiplexers. Although Fig. 1 shows an external LFSR, the same design can still be used with internal LFSR using the constraint that two bits can be swapped with each other if the output of one bit directly feeds the input of the other.



Embedding the Bit Interchanging Module with the modified clock LFSR makes the design more power efficient. Here I was implemented 3-Bit Modified LFSR. The Architecture of 3-Bit modified LFSR is shown in figure 4.3.



In this architecture the CL block contains the XOR and AND logic for controlling the clock as shown in Figure 4.1. The output from the LFSR is passed to the bit inter-changing

module which constitutes of multiplexers. It interchanges the bits as per the proposed methodology and finally generates a set of reordered test vectors

IV. EXPERIMENTAL RESULTS & ANALYSIS

Test vectors are actually the same but their order of scan shifting changes. The THD reduction obtained with maximal length 3-Bit LFSRs is

THD without order - 11
THD with order - 9

LFSR	THD without order	THD with order	THD Reduction (%)
3-bit	11	9	18
4-bit	31	24	23
5-bit	76	56	26

V. CONCLUSION

The proposition is an attempt to invoke research on the test pattern generator itself. The techniques available so far have focused upon reducing the switching activity from the test patterns generated from the generator. Embedding the switching activity minimizing techniques with a power efficient test pattern generators will be a good step ahead. Therefore a modification is proposed in the conventional LFSR by embedding it with control logic module and bit interchanging module. This culminates into a novel architecture of the test pattern generator (TPG). The modified TPG architecture is capable of not only disabling the switching units for a particular time frame but also reorders the test vectors so as to reduce the transition activity. The benefit of the proposed TPG is that it can be used with any other low power technique to have further reduction in power.

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